REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

Before addressing the substantative ground of rejection raised in the Final Rejection dated December 16, 2003, applicants have amended independent Claims 1, 49 and 50 to positively recite that the annealing step is carried out until tile or divot defects present at a top surface of said superficial Si-containing layer are reduced so as to allow optical detection of any other defect that has a lower density than the tile or divot defect. Support for this amendment to Claims 1, 49 and 50 is found throughout the specification of the present invention; see, for example, Page 3, lines 6-29. Applicants have further amended Claims 1, 49 and 50 to positively recite a step of optically detecting said other defects. Support for this amendment to the claims is found at Page 3, lines 6-29, Page 7, lines 7-14, and Page 12, lines 14-21.

Since the above amendments to the claims do not introduce any new matter into the instant application, entry thereof is respectfully requested.

In the Final Rejection dated December 16, 2003, Claims 1-22, 25-36, 40 and 48-50 stand rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of U.S. Patent No. 6,090,689 to Sadana, et al. ("Sadana '689"), U.S. Patent No. 5,534,446 to Tachimori, et al. ("Tachimori, et al.") and U.S. Patent No. 5,930,643 to Sadana, et al. ("Sadana '643").

Applicants respectfully submit that the claimed methods are not rendered obvious from the combined disclosures of Sadana '689, Tachimori, et al., and Sadana '643 since

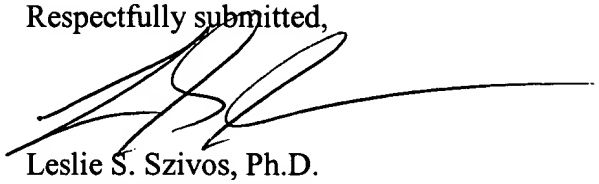
none of the prior art methods teach or suggest a method in which annealing is carried out until tile or divot defects present at a top surface of said superficial Si-containing layer are reduced so as to allow optical detection of any other defect that has a lower density than the tile or divot defect, and then optically detecting said other defects.

Applicants observe that Sadana '689, Tachimori, et al. or Sadana '643 do not teach or suggest that their annealing process is performed until tile or divot defects present at a top surface of said superficial Si-containing layer are reduced so as to allow optical detection of any other defect that has a lower density than the tile or divot defect, and then optically detecting said other defects. Indeed, each of the applied reference fails to mention that the presence of tile or divot defects and thus they could not have recognized that such defects cause a problem in optically detecting other defects that have a lower defect density than the tile or divot defects. In the claimed methods, applicants have performed the annealing step until the tile and divot defects are reduced and then they can optically measure the other defects that have a lower defect density than the tile or divot defects. Hence, the method of the present invention provides a SOI substrate that has fewer defects, especially tile and divot defects, on the top Si-containing surface which permits the detection of other defects that have an even smaller defect density than the tile or divot defects.

Based on the above amendments and remarks the rejection to the claims under 35 U.S.C. §103 have been obviated; therefore reconsideration and withdrawal of the instant rejection are respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,



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